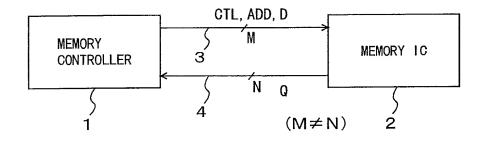
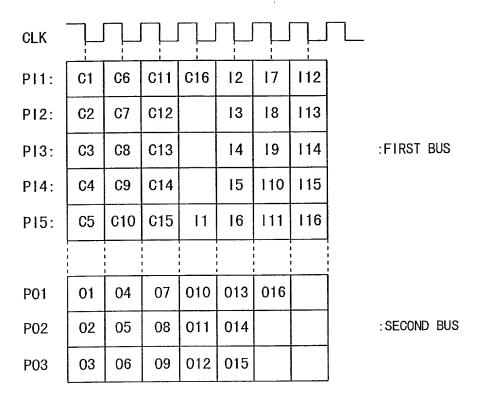
F I G. 1



F I G. 2

< COMMAND PACKET >					DATA PACKET				! !	
	C1	C 5	С9	C13	11	15	19	113	:	PI1
	C2	C6	C10	C14	12	16	110	114	:	PI2
	С3	С7	C11	C15	13	17	111	I 15	:	P13
	C4	C8	C12	C16	14	18	112	116	:	PI4
									:	CLK

FIG. 3



F | G. 4 14 11 **READ** COMMAND CONTROL CIRCUIT 6 **DECODER** WRITE PIG 13 BIT-WIDTH ROW-RELATED INPUT EXPANSION CIRCUIT CIRCUIT **BUFFER** M P 10 12 COLUMN-READ MEMORY RELATED **POG** CELL ARRAY CIRCUIT BIT-WIDTH OUTPUT REDUCTION CIRCUIT **BUFFER** 16 15 2

F | G. 5

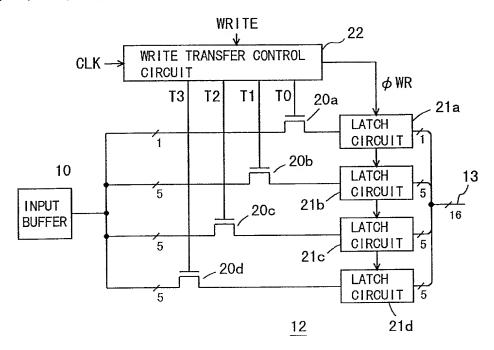


FIG. 6

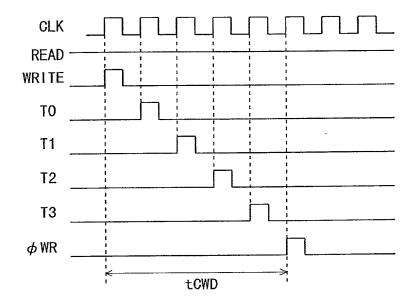


FIG. 7A

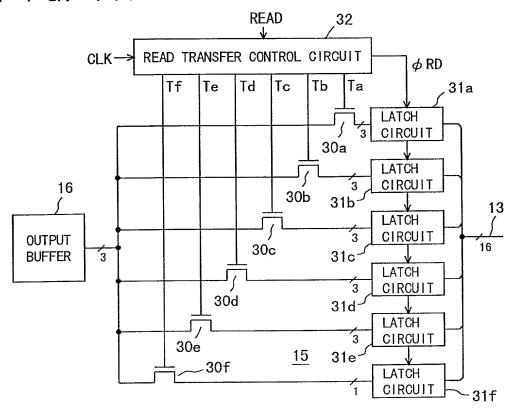


FIG. 7B

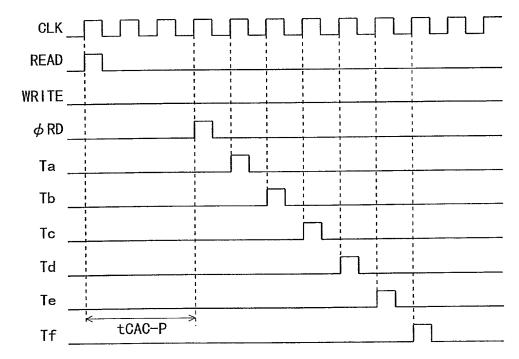
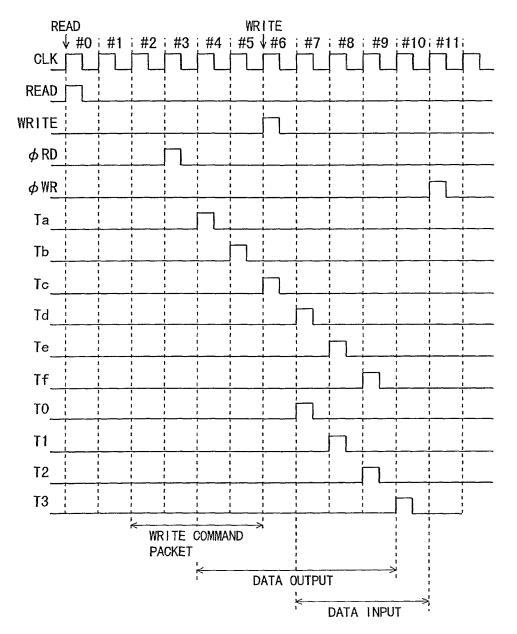


FIG. 8



F I G. 9

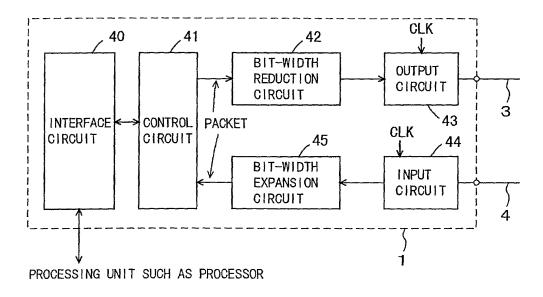


FIG. 10

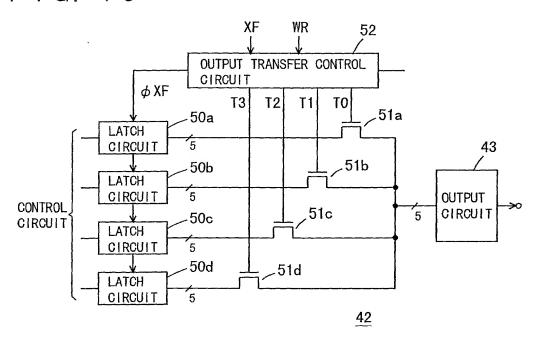


FIG. 11

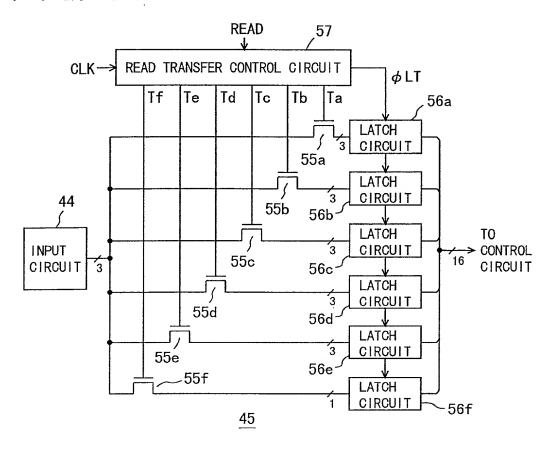


FIG. 12

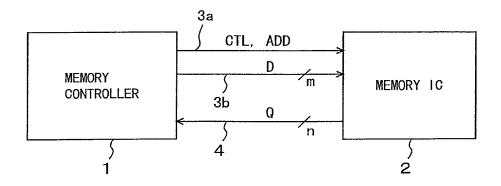


FIG. 13

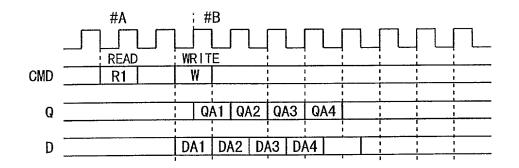
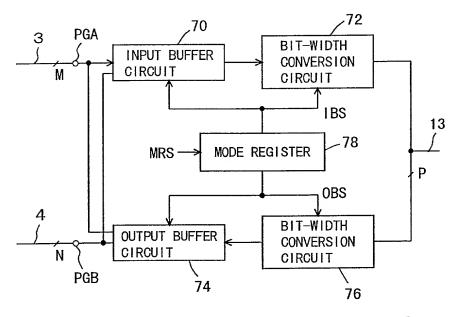


FIG. 14



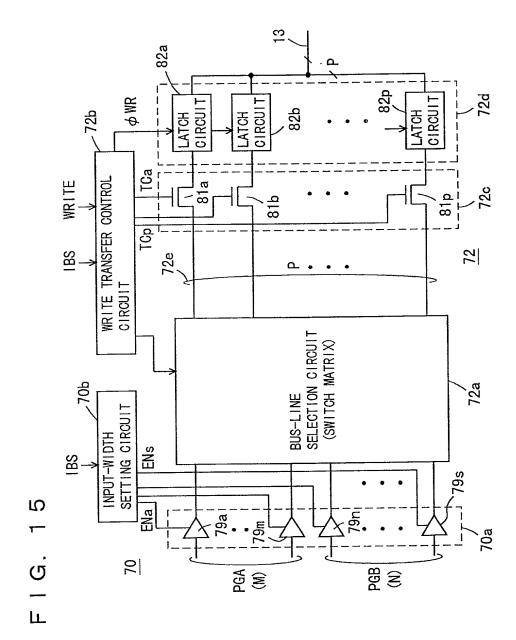


FIG. 16

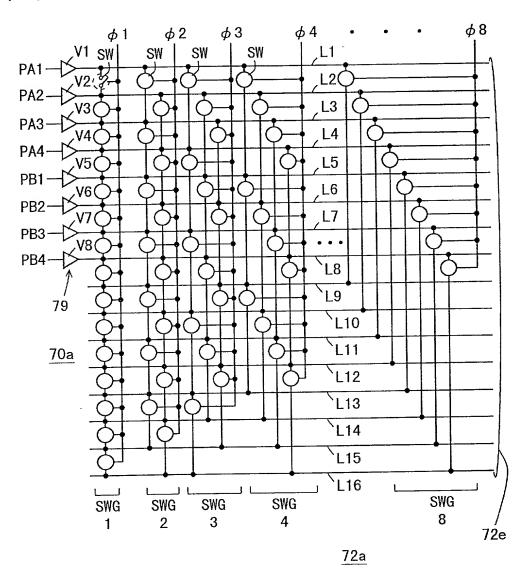


FIG. 17

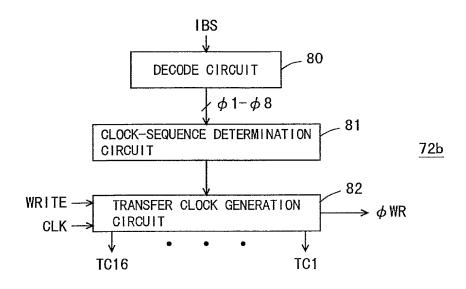
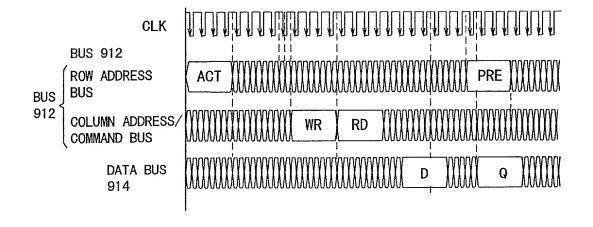


FIG. 23 PRIOR ART



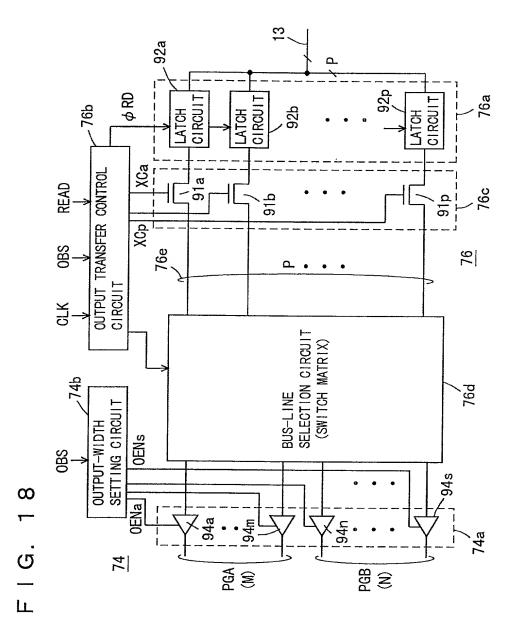
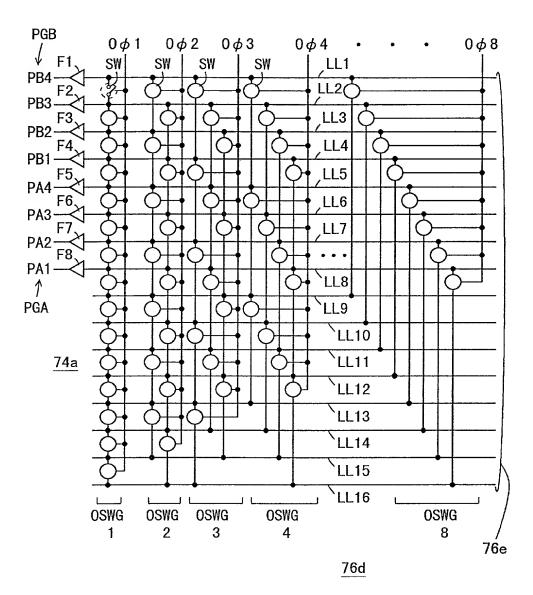
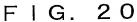
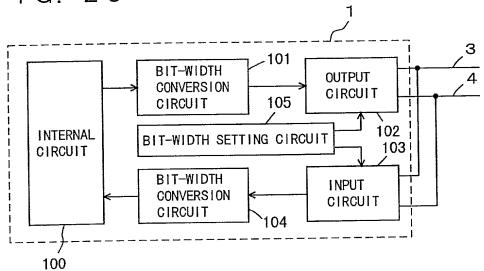


FIG. 19







F I G. 2 1 PRIOR ART

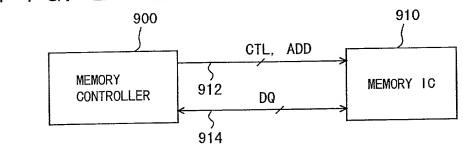


FIG. 22 PRIOR ART

